CLAIMS

Now, therefore, the following is claimed:

1. A processor purging system, comprising:

a translation lookaside buffer (TLB) having a plurality of translation pairs;

at least one memory cache; and

logic configured to detect whether at least one of the translation pairs corresponds to a purge signal, the logic further configured to assert a purge detection signal indicative of whether at least one translation pair corresponds to the purge signal and to determine, based upon the purge detection signal, whether to search the memory cache for a translation pair corresponding to the purge signal.

2. The system of claim 1, wherein the logic is further configured to purge the translation pair from the memory cache if the translation pair corresponds to the purge signal.

3. The system of claim 2, wherein the memory cache further comprises an instruction queue.

4. The system of claim 3, wherein the memory cache further comprises a mini-TLB.

5. The system of claim 2, further comprising compare logic configured to compare the purge signal with each translation pair and assert a match signal corresponding to each of the plurality of translation pairs if the purge signal corresponds to one of the translation pairs, the logic further configured to deassert the match signal corresponding to each of the plurality of translation pairs if the purge signal does not match one of the translation pairs.

6. The system of claim 5, wherein the logic is further configured to collapse the match signals corresponding to each of the plurality of translation pairs into the purge detection signal indicative of whether at least one of the translation pairs corresponds to the purge signal.

7. The system of claim 6, wherein the logic comprises a plurality of tiered logical AND gates configured to collapse the plurality of signals into the signal indicative of whether at least one of the translation pairs corresponds to the purge signal.

8. The system of claim 7, wherein the logic comprises a plurality of tiered logical OR gates configured to collapse the plurality of signals into the signal indicative of whether at least one of the translation pairs corresponds to the purge signal.

9. A computer readable medium having a program, the program comprising:

logic configured to detect whether at least one of a plurality of translation pairs in a translation lookaside buffer (TLB) corresponds to a purge signal; and

logic configured to assert a purge detection signal indicative of whether at least one of the translation pairs matched the purge signal.

10. The computer-readable medium of claim 9, wherein the program further comprises:

logic configured to compare the purge signal with each translation pair of the TLB; and

logic configured to assert a match signal for each translation pair of the TLB indicative of whether the translation pair corresponding to the matched signal matched the purge signal.

11. A processor purging system, comprising:

a translation lookaside buffer (TLB) having a plurality of translation pairs;

means for determining whether at least one of the translation pairs corresponds to a purge signal; and

means for purging components of the processor based upon the determination of whether at least one of the translation pairs corresponds to a purge signal.

12. A method for purging a processor, comprising the steps of:

detecting whether at least one of a plurality of translation pairs in a translation lookaside buffer (TLB) corresponds to a purge signal; and

asserting a purge detection signal indicative of whether a translation pair matched the purge signal.

13. The method of claim 12, wherein the detecting step further comprises the steps of:

comparing the purge signal with each translation pair of the TLB; and

asserting match signals for each translation pair of the TLB indicative of whether the translation pair corresponds to the match signal.

14. The method of claim 13, wherein the asserting a purge detection signal step further comprises the step of collapsing each match signal into a single purge detection signal indicative of whether at least one of the translation pairs matched the purge signal.

15. The method of claim 14, further comprising the step of deleting each translation pair in the TLB that matches the purge signal.

16. The method of claim 15, further comprising purging processor components resident on the processor if the purge detection signal indicates that at least one translation pair in the TLB matches the purge signal.

17. A processor purging method, comprising:

detecting whether at least one translation pair in a plurality of translation pairs within a translation lookaside buffer (TLB) corresponds to a purge signal;

asserting a purge detection signal indicative of whether at least one of the translation pairs corresponds to the purge signal; and

determining, based upon the purge detection signal, whether to search the memory cache for a translation pair corresponding to the purge signal.

18. A processor purging system, comprising:

a collection of translation pairs;

at least one memory cache;

means for asserting a purge detection signal indicative of whether at least one translation pair corresponds to a purge signal; and

means for determining, based upon the purge detection signal, whether to search the memory cache for the at least one translation pair corresponding to the purge signal.

19. A system for purging a processor, comprising:

a plurality of translation pairs;

means for detecting whether at least one of the plurality of translation pairs corresponds to a purge signal; and

means for asserting a purge detection signal indicative of whether a translation pair matched the purge signal.

20. The system of claim 19, further comprising means for determining, based upon the purge detection signal, whether to search a memory cache for a translation pair corresponding to the purge signal.